Remarks

Claims 1-18 are pending in the application and are rejected.

Claim rejections

Section 102

Claim 1-18 were rejected under 35 USC 102(e) as being anticipated by Favor (US 6,732,236). The Applicant respectfully traverses. Favor cannot support the asserted rejection for at least the reason that Favor does not disclose "if the execution of the first instruction generates a cache miss, associating the first instruction with the cache miss" as recited in independent claim 1. Further, Favor does not disclose "association logic to form an association between a cache miss and an instruction generating the cache miss" as recited in independent claims 5 and 16. Moreover, Favor does not disclose "generating a cache miss in a processor" and "assigning an identifier to the cache miss and writing the identifier in a field of a load instruction generating the cache miss," as recited in independent claim 10. Favor is further silent as to "in a processor, enqueuing a plurality of instructions needing re-execution due to respective cache misses in a re-execution queue" and "associating each instruction in the queue with a respective corresponding cache miss," as recited in independent claim 13.

In Favor, associations are never formed between instructions and cache misses generated by the instructions, as required by the present claims. In particular, in Favor there is no association formed upon the occurrence of a cache miss. See, e.g., col. 3, lines 37-43. On a cache miss, if an access request is a load, the "data is read from an appropriate target and returned directly back to" a requesting executing unit, and a cache fill is performed.

The Examiner contends that "it is clear that Favor teaches when there is a cache miss, the cache miss is stored in a retry queue to be retried when the data is ready ... ." The Applicant respectfully disagrees. If a subsequent access request needs the data from the cache fill, but the cache fill is still pending, the subsequent access request may be placed in a "Retry Request Queue" (RRQ). However, the access request to the pending cache fill is a cache *hit*, not a cache miss. See col. 3, lines 55-60:

"In this case, the lookup module 306 decodes the new access request and accesses the cache tag for the new access request in the cache tag array 316. The address lookup module 306 then determines that the access request **does hit** in the cache, but the state of the cache line is busy due to the pending cache fill."

(Emphasis added.)

Accordingly, Favor cannot meet the recitations of the present claims. Withdrawal of the asserted rejection is therefore respectfully requested.

Conclusion

In light of the above discussion, Applicant respectfully submits that the present application is in all aspects in allowable condition, and earnestly solicits favorable reconsideration and early issuance of a Notice of Allowance.

The Examiner is invited to contact the undersigned at (202) 220-4323 to discuss any matter concerning this application. The Office is authorized to charge any fees related to this communication to Deposit Account No. 11-0600.

Respectfully submitted,

Dated: MAY 25 2006

By: _____
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